METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR AND METOD OF MAKING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a metal oxide semiconductor field effect transistor, and more particularly to a metal oxide semiconductor with a lightly doped drain structure and a method of making the same.

2. Description of the Prior Art

As well-known in the technical field, such a metal oxide semiconductor field effect transistor (MOSFET) with a lightly doped drain (LDD) structure is adapted to utilize the following effects: That is, when a given voltage is applied to a gate, a channel region is defined between a source region and a drain region, so that electrons move from the source region to the drain region along the channel region.

A most typical method of making such a prior art MOSFET with a LDD structure will now be described, in conjunction with FIGS. 1A to 1C.

FIGS. 1A to 1C are cross-sectional views illustrating a method of making a MOSFET with a conventional LDD structure. As shown in FIG. 1A, a gate oxide film **22** is grown over the entire surface of a p type silicon substrate **21**.

An implantation of p type channel ions is achieved at regions including a channel region, so as to control a threshold voltage and particularly suppress a threshold voltage of a punch through possibly occurring along with a short channel.

On the gate oxide film **22**, a polysilicon layer is formed, as shown in FIG. 1B. By patterning the polysilicon layer, a gate **23** is formed. For the LDD structure, low concentration n (n^-) type source and drain regions **24** and **24***a* are then formed using a method of implanting low concentration n type ions and using the gate **23** as a mask.

Thereafter, an oxide film is formed using a chemical vapor deposition (CVD) method, as shown in FIG. 1C. The oxide film is then etched back to form side wall oxide films **25** and **25***a* at opposite side walls of the gate **23**.

High concentration n (n^+) type source and drain regions **26** and **26***a* are then formed using a method of implanting high concentration n type ions and using the gate **23** and the gate side wall oxide films **25** and **25***a* as a mask. Thus, a MOSFET with the above-mentioned LDD structure is obtained as shown in FIG. 1C.

The characteristic of the MOSFET having the LDD structure shown in FIGS. 1A to 1C is that low concentration p type (p^-) ions implanted in the entire surface of an active region of the p type silicon substrate **1** serve to control a threshold voltage and avoid an occurrence of bulk punch through.

Referring to FIG. 2, there is illustrated another MOSFET with a conventional LDD structure. The structure is the same as that of FIGS. 1A to 1C, except for a low concentration p type region **27**. Accordingly, a description of a method for making the structure will be omitted.

In the structure of FIG. 2, this low concentration p type region **27** serves to avoid an occurrence of bulk punch through.

Referring to FIG. 3, there is illustrated another MOSFET with a conventional LDD structure. The structure is the same as that of FIGS. 1A to 1C, except that a low concentration p type region **28** is formed at a portion of a bulk substrate beneath a gate. The substrate bulk corresponds to the channel region. Accordingly, a description of a method for making the structure will be omitted.

In the structure of FIG. 3, this low concentration p type region **28** serves to control the threshold voltage and avoid an occurrence of bulk punch through. This technique has been proposed in the Korean Patent Application No. 91-7881, which is co-pending as U.S. patent application 07/883,857, filed May 15, 1992.

However, the above-mentioned prior art devices have the following problems.

First, in case of the structure shown in FIG. 1C, the low concentration p type region is presented throughout the entire active region, thereby causing a junction capacitance to substantially increase. Since a potential barrier at the channel region is totally very high, the mobility of electrons from the source region to the drain region is therefore greatly reduced.

Second, in case of the structure shown in FIG. 2, the junction capacitance is also very high, in that the entire low concentration p type region is bonded to the low and high concentration n type source/drain regions. Since the channel region does not include the low concentration p type region, it is difficult to avoid an occurrence of bulk punch through at that region.

Third, in case of the structure shown in FIG. 3, since the low concentration p type region is located at the center portion of the channel region and extends from the surface of the p type silicon substrate toward the bulk, it thereby causes the potential barrier at that region to be very high. As a result, the mobility of electrons is reduced.

Generally, the punch through phenomenon means an interconnection between source and drain regions without any channel region when a given voltage is applied to those regions. Such a punch through can refer to either a surface punch through and a bulk punch through. On the other hand, the threshold voltage means the critical value of a gate voltage making it possible to conduct a current between source and drain regions. The level of the threshold voltage is controlled by an implantation of low concentration p type ions (namely, a channel ion implantation). In this case, such a channel ion implantation is carried out for controlling the threshold voltage, so as to avoid an occurrence of punch through.

SUMMARY OF THE INVENTION

Therefore, an object of the invention is to provide a MOSFET with a LDD structure capable of avoiding an occurrence of punch through at the bulk portion of a substrate and a method of making the same.

Another object of the invention is to provide a MOSFET with a LDD structure capable of reducing the junction capacitance and a method of making the same.

Another object of the invention is to provide a MOSFET with a LDD structure capable of improving a mobility of electrons in the channel region.

In one aspect, the present invention provides a metal oxide semiconductor field effect transistor comprising: a semiconductor substrate of a first conductivity type; a gate located on said substrate; a channel region of the first conductivity type located beneath a surface portion of the substrate corresponding to a region defined be-